REMARKS

Claims 1 through 16 and 26 through 39 are currently pending in the application.

Claims 17 through 25 and 40 through 50 have been canceled.

This amendment is in response to the Final Office Action of May 8, 2002 and the Advisory Action of July 25, 2002.

Applicant submits herewith, under cover of a separate Letter to the Chief Draftsman, for proposed addition of FIG. 3A to the drawings. Applicant respectfully requests approval of the corrections to the drawings and will file corrected formal drawings upon receipt of such approval and a Notice of Allowance and Issue Fee Due in the application.

Claims 1 through 4 and 26 through 29 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Eide (U.S. Patent 5,313,096) in view of Kohno et al. (U.S. Patent 5,293,068).

Claims 5, 6, 30 and 31 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Shen (U.S. Patent 5,384,689) in view of Kohno et al. (U.S. Patent 5,293,068).

Claims 8 through 11 and 33 through 36 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Kryzaniwsky (U.S. Patent 5,099,309) in view of Kohno et al.

Claims 12, 14 through 16, 37 and 39 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Kryzaniwsky in view of Kohno et al. and Shen.

Claims 7 and 32 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Shen and Kohno as applied to claims 5 and 30 above, and further in view of Degani et al. (U.S. Patent No. 5,473,512).

Claims 13 and 18 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Kryzaniwsky, Kohno and Shen as applied to claims 12 and 37 above, and further in view of Degani et al.

After carefully considering the cited prior art, the rejections, and the Examiner's comments, Applicant requests reconsideration of the application in view of the arguments set forth below.

Applicant further submits that to establish a *prima facie* case of obviousness under 35 U.S.C. § 103 three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Third, the cited prior art reference must teach or suggest all of the claim limitations. Furthermore, the suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicant's disclosure.

After carefully considering the Examiner's comments in the Advisory Action mailed on July 25, 2002, Applicant requests reconsideration of Claims 1-11, 13, 17-36, and 38 in view of the new arguments set forth below.

Applicant submits that Examiner's rejection of Claims 1-4 and 26-29 is based upon an incorrect combination of prior art and should be withdrawn.

To establish a *prima facie* case of obviousness under 35 U.S.C. § 103 three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Third, the cited prior art reference must teach or suggest all of the claim limitations. Furthermore, the suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicant's disclosure.

Turning first to Claims 1 through 4 and 26 through 29, which were rejected under 35 U.S.C. § 103(a) as being unpatentable over Eide (U.S. Patent 5,313,096) in view of Kohno et al. (U.S. Patent 5,293,068). Applicant submits that there is no suggestion or motivation to combine the Eide and Kohno references to establish a *prima facie* case of obviousness under 35 U.S.C. § 103. In fact, the Eide reference teaches away from the combination. At column 2, lines 25-28, the Eide reference states; "[b]ecause the chip terminals are wire bonded inwardly through apertures in the lower substrate layer, such wire bonding is confined within the outer periphery of the chip,"

and at column 6, lines 48-51, the Eide reference states "[T]he manner in which inward bonding through the apertures 38 and 40 provides for increased chip density in accordance with the invention can be better appreciated." It is stated that it would have been obvious to use the teachings of Kohno regarding bond pads along a longitudinal axis to modify Eide, but the repeated reference to bonding from the periphery of the die inward clearly teaches away from an implementation where it would be desirable to form the bond wires outward toward the chip periphery. It is improper to combine references where the references teach away from their combination. *in re Graselli,* 713 F.2d 731, 743, 218 USPQ 769, 779 (Fed Cir. 1983).

Furthermore, when modifying one piece of prior art with another to arrive at the conclusion that the combination is obvious, "the proposed modification cannot render the prior art unsatisfactory for its intended purpose." MPEP 2143.01. A major object of Eide is to eliminate the waste of space among semiconductors attached to a substrate. Eide specifically rejects the "outward" lead configuration of Fig. 9, in favor of his own "inward" lead configuration (Fig. 10) which "provides for substantially greater chip density within the chip stack." Col. 6, Line 68. Taking the idea of axial bond pad placement from Kohno would inevitably lead to the space-inefficient "outward" lead configuration. Therefore, the combination of Eide and Kohno should be considered improper and cannot establish a *prima facie* case of obviousness under 35 U.S.C. § 103.

While applicant gratefully acknowledges Examiner's suggestion to include, in Claims 1 and 26, language affirming the outward direction of the leads, such is present in the existing structure of the semiconductor die when the bond pads of the semiconductor die extend along an axis thereof. Accordingly, Claims 1 and 26 are allowable. With regard to Claims 2 through 4, applicant acknowledges the arguments in the Office Action concerning Eide disclosing attachment methods and filling of vias in the substrate. However, since these claims are dependent on allowable Claim 1, they should be allowable. For the same reason, Claims 26-29 should allowable as dependent on Claim 26.

Next, turning to Claims 5, 6, 30 and 31, which were rejected under 35 U.S.C. § 103(a) as being unpatentable over Shen (U.S. Patent 5,384,689) in view of Kohno et al. (U.S. Patent 5,293,068), Applicant respectfully submits that Shen and Kohno cannot be combined to arrive at Applicant's invention. From the language of Applicant's Claims 5 and 30, it is clear that the die is above the "board" which is, in turn, above the masterboard. The board has two surfaces or faces which are connected by via structures (i.e., the faces are on opposite sides of the board). Thus, the die and the masterboard, when assembled according to applicant's claims, attach to opposite sides of the board. The advantage of this configuration is, as pointed out in the specification, to have a midpiece which acts as a physical and electrical adaptor between dies and masterboards that are otherwise unmatched due to odd sizes and electrical configurations.

Shen, on the other hand definitely contemplates an arrangement in which the die itself is up against the masterboard, covered and surrounded by printed circuit board. The upper printed circuitboard is referred to as "top" throughout. (It is also suggested that this "top" surface be coated with a plastic protective layer. Col. 3 Line 25.) Not only are advantages of Applicant's process lost in Shen's process, but the processes are so different that combining Shen with Kohno will not equal Applicant's invention.

In addition, Applicant believes the issue has not been addressed that while Shen makes an oblique reference, at column 3, lines 19-24, to mounting "to another printed circuit board (not shown) by conventional surface mounting techniques," this certainly does not suggest an attachment and connection method to a master board. Rather, it merely suggests that a connection is possible. Shen says nothing more about this connection and the connection could not be made using "conventional surface mounting techniques" without additional steps and additional elements not disclosed in Shen. Further, nothing in Kohno teaches anything about connections to a master board. Consequently, as it relates to connections to a master board, the addition of Kohno would not advance the obviousness argument to establish a *prima facie* case of obviousness under 35 U.S.C. § 103. Solely Applicant's disclosure contains a suggestion for a method of attachment and connection. Given the above arguments, Applicant continues to submit

that there is no suggestion or motivation to modify Shen within the combination of Shen and Kohno, or the combination of Shen with knowledge generally available to one of ordinary skill in the art. Accordingly, Claims 5 and 30 are allowable. Claims 6 and 31, are also allowable as claims dependent on allowable independent claims 5 and 30, respectively.

Next, turning to claims 8 through 11 and 33 through 36, which were rejected under 35 U.S.C. § 103(a) as being unpatentable over Kryzaniwsky (U.S. Patent 5,099,309) in view of Kohno et al. Applicant submits that there is no suggestion or motivation to combine the Kryzaniwsky and Kohno references to establish a *prima facie* case of obviousness under 35 U.S.C. § 103. Kryzaniwsky does not disclose the element of attaching the surface having a plurality of pads thereon of a semiconductor die of the at least two semiconductor die to the die surface of the substrate. Instead, referring to figures 1A – 1L in Kryzaniwsky, the die is attached from below to a thermal conductor plane (1) with thermally conductive dielectric tape (34). According to the Kryzaniwsky reference at column 3, lines 35 through 37, the layer adjacent to the surface having the bonding pads (40) is laminated **over** the chip core structure (emphasis added). This implies attachment of the adjacent layer to the dielectric material (11) rather than the die. Further, nothing in Kohno teaches anything about attaching the surface having bond pads to any kind of substrate. Consequently, as it relates to attaching the die surface having bond pads to a substrate, the addition of Kohno does not advance the obviousness argument to establish a *prima facie* case of obviousness under 35 U.S.C. § 103. Therefore, Applicant submits that there is no suggestion or motivation to modify Kryzaniwsky within the combination of Kryzaniwsky and Kohno, or the combination of Kryzaniwsky with knowledge generally available to one of ordinary skill in the art. Accordingly, claims 8 and 33 are allowable. Claims 9 through 11 are also allowable as dependent claims of the now allowable independent claim 8. Similarly, claims 34 through 36 are allowable as dependent claims of the now allowable independent claim 33.

Additionally, Claims 8 and 33 have been amended to draw further distinction between Applicant's process and the process of Kryzaniwsky. The following words have been added to the ends of the claims: "the second attachment surface retaining unused bond pads for the at least

two semiconductor die to have the ability for electrical connection with an electrically conductive device connected to said pads." The change underscores a function of the substrate, namely to act as an adaptor.

Next, addressing Claims 12, 14 through 16, 37 and 39, which were rejected under 35 U.S.C. § 103(a) as being unpatentable over Kryzaniwsky in view of Kohno et al. and Shen. Applicant submits that there is no suggestion or motivation to combine the Kryzaniwsky, Kohno, and Shen references to establish a prima facie case of obviousness under 35 U.S.C. § 103. Kryzaniwsky does not disclose the element of attaching each semiconductor die of the plurality of semiconductor die to a portion of the die side surface of the board. Instead, referring to figures 1A – 1L in Kryzaniwsky, the die is attached from below to a thermal conductor plane (1) with thermally conductive dielectric tape (34). According to the Kryzaniwsky reference at column 3, lines 35 through 37, the layer adjacent to the surface having the bonding pads (40) is laminated **over** the chip core structure (emphasis added). This implies attachment of the adjacent layer to the dielectric material (11) rather than the die. Further, nothing in Kohno teaches anything about attaching the surface having bond pads to any kind of substrate. Consequently, as it relates to attaching the die surface having bond pads to a substrate, the addition of Kohno does not advance the obviousness argument to establish a prima facie case of obviousness under 35 U.S.C. § 103.

Similarly, the Shen reference cannot be combined with Kryzaniwsky to support an obviousness rejection for the element of attaching each semiconductor die of the plurality of semiconductor die to a portion of the die side surface of the board. Shen contains nothing about attaching the die to the die side surface of the board. Applicant submits that the method for holding the die in place in the die receiving cavity is not expressed or implied within the Shen reference. The Shen reference states simply, at column 3, lines 7 and 8, that the die is "received in the die-receiving cavity." Furthermore, where Shen desires an attachment, "between the upper and lower printed circuit boards," it is expressly defined at column 3, lines 3 through 5.

To support a rejection that the element of attaching each semiconductor die of the plurality of semiconductor die to a portion of the die side surface of the board based upon Kryzaniwsky in

light of Shen, an improper obviousness position of a to try rationale would be required. "What would have been 'obvious to try' would have been to vary all parameters to try each of numerous possible choices until one possibly arrived at a successful result, where the prior art gave either no indication of which parameters were critical or no direction as to which of may possible choices is likely to be successful." In re O'Farrell, 853 F.2d 894, 903, 7 USPQ2d 1673, 1681 (Fed. Cir. 1988). In the Shen reference, the die may be held in place by any number of alternate means and none is suggested. For example, a press fit or other attachment mechanism to the inner peripheral wall (71) of the lower printed circuit board would hold the die in place. Or, the combination of bond pads and protective layer may hold the die in place. Or possibly more significantly, the Shen reference states at column 3, lines 8 through 10 that the "lower surface of the die is substantially flush with the bottom surface of the lower printed circuit board." One could therefore use an additional plate upon which the lower surface of the die and the bottom surface of the lower printed circuit board are attached, similar to Kryzaniwsky. Many more alternative attachment mechanisms could be tried.

Additionally, Applicant respectfully submits that the combination of Kryzaniwsky, Kohno, and Shen does not suggest the element, in Claims 12 and 37, of connecting the board and master board using said plurality of electrical connectors on said board to said plurality of circuit traces on said master board to establish a prima facie case of obviousness under 35 U.S.C. § 103. As pointed out in the Office Action, Shen makes an oblique reference, at column 3, lines 19-24, to mounting "to another printed circuit board (not shown) by conventional surface mounting techniques." While this may suggest a connection to a master board is possible, it certainly does not suggest an attachment or connection elements. Shen says nothing more about this connection and the connection could not be made using "conventional surface mounting techniques" without additional steps and additional elements not disclosed or implied in Shen. Further, nothing in Kohno, or Kryzaniwsky teaches anything about connections to a master board. Consequently, as it relates to connections to a master board, the addition of Kohno and Kryzaniwsky does not advance the obviousness argument to establish a prima facie case of obviousness under 35 U.S.C.

§ 103. Solely Applicant's disclosure contains a suggestion for a method of attachment and connection.

Therefore, Applicant submits that there is no suggestion or motivation to modify Kryzaniwsky within the combination of Kryzaniwsky, Kohno, Shen, or knowledge generally available to one of ordinary skill in the art to establish a prima facie case of obviousness under 35 U.S.C. § 103. Accordingly, claims 12 and 37 are allowable. Claims 14 through 16 are also allowable as dependent claims of the now allowable independent claim 12. Similarly, claim 39 is allowable as a dependent claim of the now allowable independent claim 37.

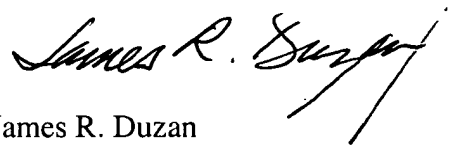
Next, turning to Claims 7 and 32, which were rejected under 35 U.S.C. § 103(a) as being unpatentable over Shen and Kohno as applied to claims 5 and 30 above, and further in view of Degani et al. (U.S. Patent No. 5,473,512). Claim 7 is allowable as a dependent claim on the now allowable independent Claim 5. Claim 32 is allowable as a dependent claim on the now allowable independent claim 30.

Finally, turning to Claims 13 and 38, which were rejected under 35 U.S.C. § 103(a) as being unpatentable over Kryzaniwsky, Kohno and Shen as applied to claims 12 and 37 above, and further in view of Degani et al. Claim 13 is allowable as a dependent claim on the now allowable independent claim 12. Claim 38 is allowable as a dependent claim on the now allowable independent claim 37.

Additionally, Applicant has amended claim 12 to correct typographical and antecedent reference errors in the claims for the consistency of usage of terminology throughout the claims.

In summary, based on the foregoing, Applicant requests the allowance of claims 1 through 16 and 26 through 39, and the case passed for issue.

Respectfully submitted,



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Enclosure: Version with Markings to Show Changes Made

N:\2269\2687.3\Second Amendment Under 37 CFR 1.116.wpd

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

Please substitute the following paragraphs for the BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS section of the specification:

While the specification concludes with claims particularly pointing out and distinctly claiming that which is regarded as the present invention, the advantages of this invention can be more readily ascertained from the following description of the invention when read in conjunction with the accompanying drawings in which:

FIG. 1 is a side view of one embodiment of the present invention;

FIG. 2 is a side view of a second embodiment of the present invention;

FIG. 2A is a top view of the second embodiment of the present invention shown in FIG. 2;

FIG. 3 is a side view of a third embodiment of the present invention; [and]

FIG 3A is an upside-down exploded perspective view of selected portions of the third embodiment; and

FIG. 4 is a side view of a fourth embodiment of the present invention.

Please substitute the following paragraph for the first full paragraph on Page 8 of the specification:

FIGs. 3 and 3A illustrate[s] a third embodiment of the present invention designated as a wire bond style/flip chip attach assembly 300. Components which are common to the previous figures retain the same numeric designation. The assembly 300 comprises an inverted semiconductor die 12 having lower surface 14 with at least one bond pad 38 on the semiconductor die lower surface 14. As illustrated, the bond pads 38 are arranged in two rows extending down the longitudinal axis of die 12 being located transverse to the plane of the page, such an arrangement commonly being used for a "leads over" connection to frame leads extending over

the die in its normal, upright position. The semiconductor die lower surface 14 is bonded to the adaptor board upper surface 20 with an insulating, sealing adhesive 40. The adaptor board 18 includes at least one or more wire bond via 42 which is located in a position or positions aligned with the semiconductor die bond pads 38. Each individual wire bond 134 is connected to each corresponding individual semiconductor die bond pad 38. Each wire bond 134 extends from the semiconductor die bond pad 38 to a corresponding bond pad or lead 39 on the adaptor board lower surface 24, which communicates with adaptor board connectors 22 through circuit traces 23. The master board terminals 31 are in electrical communication with at least one adaptor board connector 22 extending substantially perpendicularly from the adapter board lower surface 24. Preferably, a sealant 44 encases the bond wires 134 and seals the wire bond via 42 to prevent contamination and damage to the wire bonds.

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

A marked-up version of each of the presently amended claims, highlighting the changes thereto, follows:

8. (Three Times Amended) A method of electrically connecting at least two semiconductor die to a substrate, comprising:

providing at least two semiconductor die, each semiconductor die being one of a semiconductor die having a surface having a plurality of bond pads extending along a longitudinal axis of said die on said surface and a semiconductor die having a surface having a plurality of bond pads extending in a leads-over configuration on said surface;

providing a substrate having a die side surface, a second attachment surface, at least two vias extending through the substrate from the die side surface to the second attachment surface, a plurality of circuits, and a plurality of bond pads located on the second attachment surface of the substrate;

attaching the surface having a plurality of bond pads thereon of a semiconductor die of the at least two semiconductor die to the die side surface of the substrate having the plurality of bond pads of the semiconductor die located over one of the at least two vias extending through the substrate; and

connecting said plurality of bond pads of the semiconductor die to said plurality of bond pads of said substrate using a plurality of wire bonds, said plurality of wire bonds extending through the one via extending through the board of the at least two vias extending through the substrate; the second attachment surface retaining unused bond pads for the at least two semiconductor die to have the ability for electrical connection with an electrically conductive device connected to said pads.

12. (Twice Amended) A method of electrically connecting a plurality of semiconductor die to a master board, comprising:

providing a plurality of semiconductor die, each semiconductor die <u>being a semiconductor die</u> having a plurality of bond pads extending along a longitudinal axis of said die on said surface and a semiconductor die having a surface having a plurality of bond pads extending in a leads-over configuration on said surface;

providing a master board having a plurality of circuit traces thereon;

providing a board having a die side surface, a second attachment surface, a plurality of vias extending through the board from the die side surface to the second attachment surface, a plurality of circuits, and a plurality of bond pads located on the second attachment surface of the board;

providing a plurality of electrical connectors for connecting the plurality of bond pads located on the second attachment surface of the board to the circuit traces of the master board;

attaching each semiconductor die of the plurality of semiconductor die to a portion of the die side surface of the board;

connecting said plurality of bond pads of each semiconductor die to said plurality of bond pads of said board using a plurality of wire bonds, said plurality of wire bonds extending through the [a] <u>plurality of</u> via<u>s</u> extending through the[n] board; and

connecting said board and master board using said plurality of electrical connectors on said board to said plurality of circuit traces on said master board.

33. (Three Times Amended) A method of attaching at least two semiconductor die to a substrate, comprising:

providing at least two semiconductor die, each semiconductor die being one of a semiconductor die having a surface having at least one bond pad extending along a longitudinal axis of said die on said surface and a semiconductor die having a surface having at least one bond pad extending in a leads-over configuration on said surface;

providing a substrate having a die side surface, a second attachment surface, at least two vias extending through the substrate from the die side surface to the second attachment surface, at least two circuits, and at least two bond pads located on the second attachment surface of the substrate;

attaching the surface having at least one bond pad thereon of a semiconductor die of the at least two semiconductor die to the die side surface of the substrate having the at least one bond pad of the semiconductor die located over one of the at least two vias extending through the substrate; and

connecting said at least one of each of the semiconductor die to said at least two bond pads of said substrate using at least two wire bonds, at least one wire bond of said at least two wire bonds extending through the one via extending through the board of the at least two vias extending through the substrate; the second attachment surface retaining unused bond pads for the at least two semiconductor die to have the ability for electrical connection with an electrically conductive device connected to said pads.